(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **63085942 A**

(43) Date of publication of application: **16 . 04 . 88**

(51) Int. Cl **G06F 11/28**
G06F 15/16

(21) Application number: **61231873**

(22) Date of filing: **30 . 09 . 86**

(71) Applicant: **TOSHIBA CORP**

(72) Inventor: **INOUE ATSUSHI**

(54) SUPPORTING DEVICE FOR DEBUGGING OF PARALLEL PROGRAM

(57) Abstract:

PURPOSE: To easily perform debugging on parallel programs, by attaching a function on a device to input a stop signal from a processor designated as the object of the debugging out of plural sets of processors, and to output a stop request signal to all of the processors designated as the objects.

CONSTITUTION: When a user inputs a binary code representing the processor number designated as the object of the debugging to a decoder 20 through a processor selection signal line 11 before executing a program, corresponding flip-flops 21W24 are set. Thereby, the selection of the processor is completed, and the execution of the programs of all of the processors are started. When the processor designated as the object of the debugging arrives at a break point, the processor outputs the stop signal Bi to a stop control part. The stop signal Bi is immediately outputted from AND gates 31W34 to an OR gate 40. The OR gate 40 outputs the stop request signal S to all of the processors. As a result, the processors not arriving the break points are stopped their operations compulsorily by the interruption of the stop request signal S.